A GAAS SINGLE CHIP 2.4 GHZ PLL FREQUENCY MULTIPLIER

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ABSTRACT

A monolithic GaAs frequency synthesizer / multiplier for the 2.4 GHz ISM band is presented. The single chip device consists of a VCO, a prescaler ÷ 16, a phase detector and a loop filter. Measured phase noise is -102 dBc/Hz at 100 kHz offset while the frequency of operation covers 2.3 GHz to 2.55 GHz . The device runs from a single 5 V supply and delivers +3 dBm of RF output power. The chip was mounted in a plastic package and a ready to use demonstrator board was designed.

INTRODUCTION

A lot of monolithic devices for wireless applications up to 2.5 GHz are now available commercially, using both GaAs-MESFET and silicon bipolar technologies. Power and low noise amplifiers as well as T/R switches are preferably realized in GaAs, whereas devices for frequency synthesis, crucial building blocks in any wireless equipment, mostly use silicon bipolar technology for its inherent lower phase noise and the higher density of digital circuitry. However, almost all of the silicon synthesizer chips for the wireless frequency bands need an external VCO and an external loop filter due to the non ideal characteristics of silicon as a substrate material. Very low cost products call for an integration of those components too, and mechanical tuned off chip elements are strictly prohibited in these applications [1,2,3].
GaAs-MESFET technology provides semi insulating substrates for low loss passive structures such as inductors and capacitors, making it possible to integrate the components in question. It is the goal of the design project presented to show the ability of standard GaAs MESFET technology to integrate a complete frequency synthesizer on a single GaAs chip without the need for any external components. In order to save cost, the frequency synthesizer should be available in a plastic package with only minor performance degradation.

CIRCUIT DESIGN

A PLL frequency multiplier with these goals in mind has been designed and realized. The chip comprises a VCO (including the resonator) for 2.4 GHz, a fixed ratio frequency divider (:16), a phase detector, a passive loop filter and some amplifiers/buffers (Fig. 1). The complete circuit is fully differential except for the push-pull output driver stage and for the loop filter.

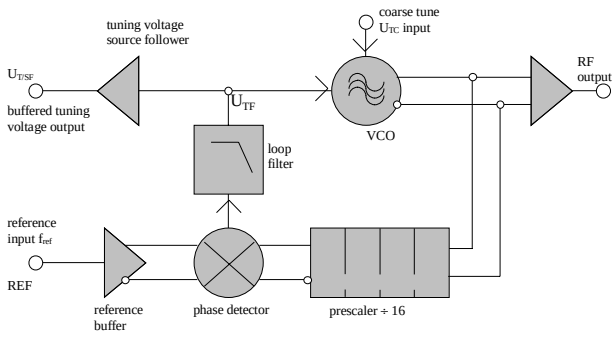

Fig. 1: Block diagram of monolithic 2.4 GHz PLL frequency multiplier

When the PLL is in lock, the VCO is held at exactly 16 times the reference frequency of about 150 MHz fed into the chip at the REF pin, and therefore the PLL acts as a multiplier. Using this high a reference frequency in conjunction with an on chip passive loop filter makes it possible to keep the loop bandwidth exceptionally high

(approx. 10 MHz). VCO phase noise is therefore suppressed over a large range of offsets, and fast frequency tuning is possible without the loop loosing lock. The actual circuit design was carried out with a time domain simulator. Simulations of the lock-in procedure indicate a settling time of some 150 ns with small overshoot.

The VCO (Fig. 2) is formed by a capacitively cross coupled differential amplifier acting as a broadband negative resistance. The VCO tank is built by an inductance L1 and a parallel capacitance C1. Two deep depletion FET (M1_1, M1_2) are connected as varactor diodes.

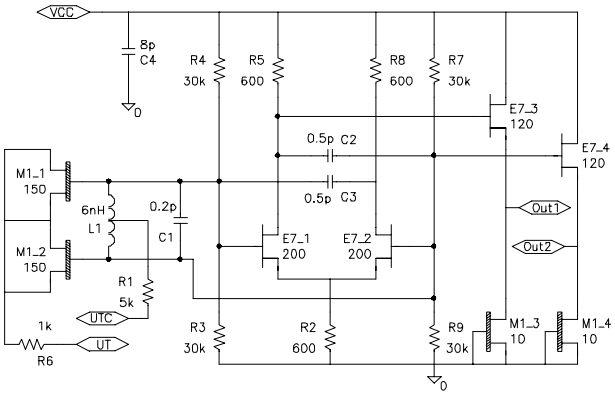

Fig. 2: Schematic of VCO with L-C parallel resonator and deep depletion FET varactor

There are two control voltage inputs to the VCO: The coarse tuning voltage UTC sets the free running frequency of the oscillator and is connected to the middle of the resonator inductance. This point is on virtual ground potential and so the externally set voltage results in no degradation of the resonator quality factor Q. The loop control voltage UT is connected to the sources of the two varactor FET via a 1 kΩ series resistor. This control voltage UT is generated by the phase detector and the loop filter (Fig. 3).

The phase detector is built by an EXOR gate [4]. The differential inputs posA/negA and posB/negB of the buffered reference frequency and the prescaled VCO frequency respectively are compared and a current proportional the their phase difference is injected into the loop filter built by R7, C2, R8 and C3. The first pole formed by R7 and C2 is responsible for the large 10 MHz loop bandwidth, while the second much higher pole helps to further suppress spurious output signals at offset frequencies at multiples of the reference frequency.

The PLL frequency multiplier is fabricated with a commercial ion implanted enhancement/depletion GaAs-MESFET process (0.7µm gate length), consuming about 2 mm^2 of GaAs real estate and 60 mA of supply current at a single 5 V supply (Fig. 4).

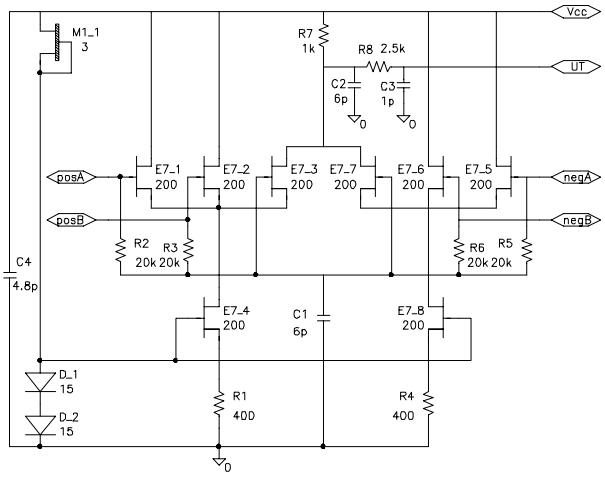

Fig. 3: Schematic of the EXOR phase detector and the passive loop filter

The packaged chip only needs 5 terminals plus ground, of which only one carries a high frequency. These include a coarse tune input to set the VCO center frequency, and a buffered control voltage output. This makes possible the use of very low cost plastic packages without degradation in performance. For prototype evaluation, a metal TO-5 and a plastic SO-14 package is used.

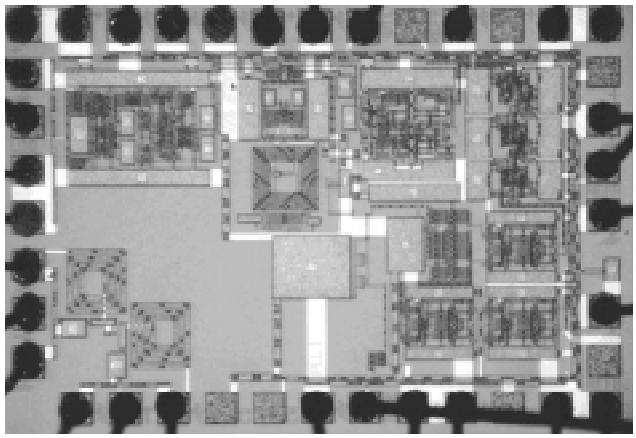

Fig. 4: Chip photograph of the 2.4 GHz PLL

MEASUREMENTS

Initially, the chip was tested in the TO-5 package using a low phase noise lab synthesizer as a reference at approx. 150 MHz, and a spectrum analyzer to watch the RF output. The VCO center frequency can be set with the

coarse tuning input UTC anywhere between 2.3 GHz and 2.5 GHz. Leaving the coarse tuning voltage fixed, a tuning range of more than 100 MHz results (Fig. 5).
As a result of the high loop bandwidth, the loop locks immediately, regardless of the current frequency of the VCO. The capture range is identical with the lock range, although the phase detector is not of the frequency sensitive type. Figure 6 shows the output frequency range of the VCO for a -5dBm reference frequency swept from 160 MHz down to 140 MHz. Locking range is more than

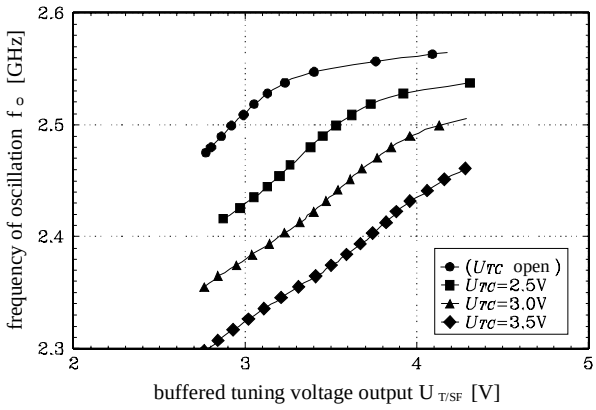

Fig. 5: Pulling behavior of VCO, measured at the buffered loop filter output, for different values of the coarse tuning voltage UTC

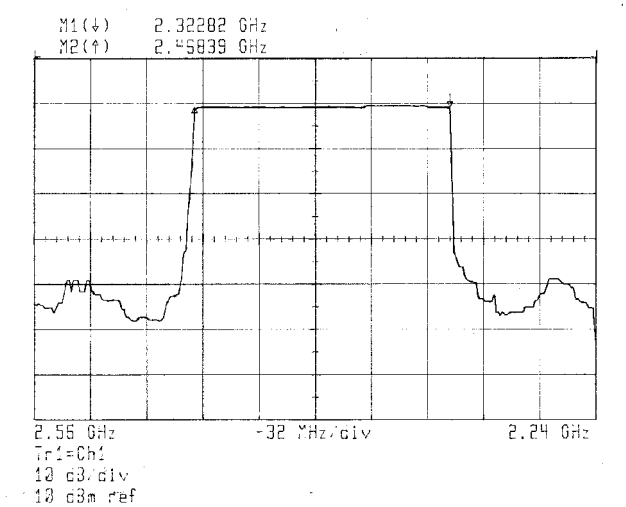

Fig. 6: Locking range of the VCO for a sweep in reference frequency from 160 MHz to 140 MHz

140 MHz with the center frequency set to 2.4 GHz. Output power measures +3dBm. This measurement was performed with a HP 70820A transition analyzer with its receiver tuned to 16 times the swept input (reference) frequency; a loss of signal on the display therefore indicates that the PLL has lost lock.

The chip was then tested in a plastic SO-14 package. A small demonstrator board was built consisting of a 155.5 MHz fundamental quartz oscillator, a voltage divider for the coarse frequency control input UTC, and the plastic encapsulated GaAs chip (Fig. 7). The demonstrator board measures 2x2 cm^2 , needs only a single +5V / 75mA supply voltage input and provides a 2.48 GHz quartz stabilized output signal with +2 dBm output power. The output spectrum is very clean, showing only low level spurious mainly at $\pm 2\, f_{ref}$ (-44 dBc), and weaker ones at $\pm\, f_{ref}$ (-60 dBc) as shown in Fig. 8. These values are slightly worse than the ones measured with the chip in the TO-5 package. The reason for the difference is suspected to be the fact, that in the plastic package no supply blocking capacitor was mounted within the package was used while in the metal can, a 100 pF chip capacitor was used.
There are several suppliers of miniaturized, low cost dielectric resonator filters with bandwidths smaller than 300 MHz. Such filters could be used to further suppress the spurious components in the output signal, if desired.

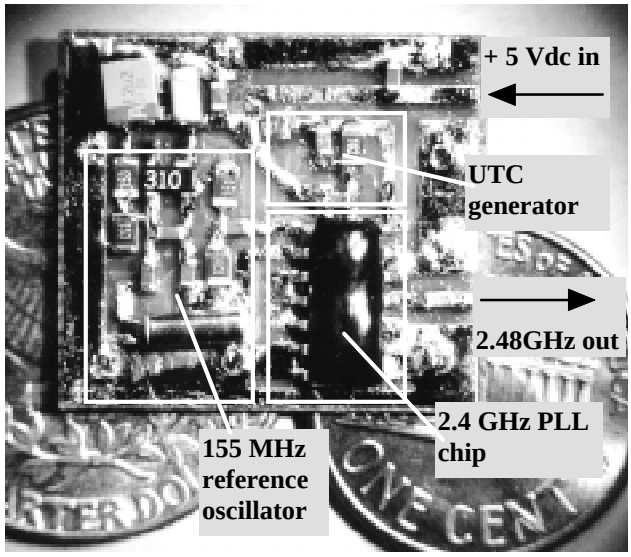

Fig. 7: Photograph of demonstrator board (actual size: 2x2 cm^2)

Phase noise performance of the demonstrator board was measured using a HP 8565E spectrum analyzer. Phase noise is -90 dBc/Hz and -102 dBc/Hz at 10 kHz and 100 kHz offset respectively (Fig. 9).

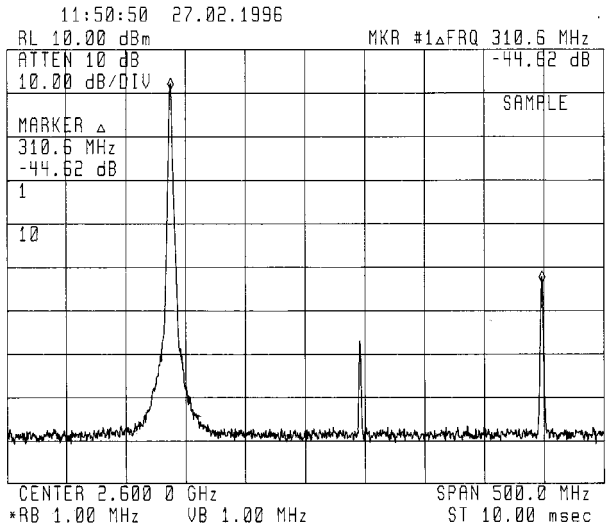

Fig. 8: Measured output spectrum of the demonstrator board (UTC= 3V)

The lock in behaviour of the PLL was simulated using the time domain simulation package PSpice. The complete circuit was simulated on transistor level. Figure 10 shows the output voltage of the phase detector and the control voltage UT after the passive loop filter.

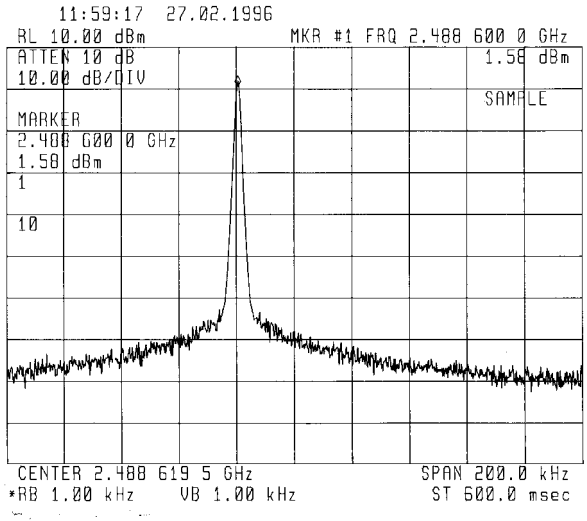

Fig. 9: Measured phase noise performance of PLL showing -90 dBc/Hz and -102dBc/Hz at 10 kHz and 100 kHz offset respectively

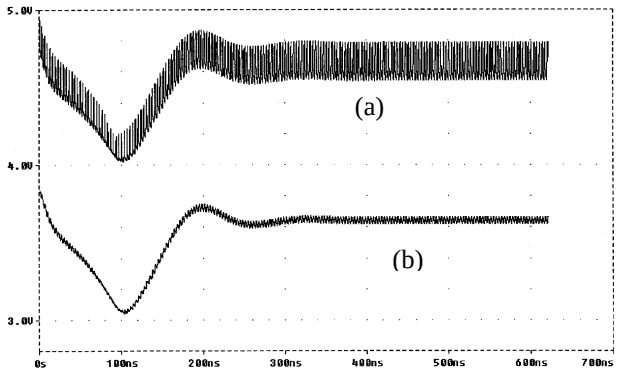

Fig. 10: Simulated lock in behaviour of PLL: (a) ouput voltage of phase detector (ploted with 1 V offset) (b) control voltage UT after loop filter

CONCLUSIONS

It was shown that monolithic frequency synthesizers for frequencies above 2 GHz can be realized with commercial GaAs-MESFET-technology. The main advantage against the silicon competition is the ability to completely integrate all components, including VCO and loop filter. This offers smaller assembly cost with commercial products, higher repeatability and no need for tuning or tweaking. Good performance in regard to phase noise and spurious is achieved, all at moderate power consumption and chip size. It is shown, that the PLL may be mounted into a plastic package with only minor performance degradation.

Acknowledgment

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